REMARKS

An Excess Claim Fee Payment Letter is submitted herewith to cover the cost of four (4) excess total claims.

Claims 11-18 and 26-31 and 33-43 are all the claims presently pending in the application. Claims 11, 26, 38 and 39 have been amended to more particularly define the invention. Claims 40-43 have been added to claim additional features of the claimed invention.

It is noted that the claim amendments are made only for more particularly pointing out the invention, and not for distinguishing the invention over the prior art, narrowing the claims or for any statutory requirements of patentability. Further, Applicant specifically states that no amendment to any claim herein should be construed as a disclaimer of any interest in or right to an equivalent of any element or feature of the amended claim.

Claims 11-12, 15-16, 18, 26, 28-29, 33-35 and 36-38 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Durlam, et al. (U.S. Patent No. 5,940,319). Claims 13-14, 17, 27 and 30-31 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Durlam, et al., in view of Bronner, et al. (U.S. Patent No. 6,242,770). Claim 39 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Durlam, et al., in view of Scheuerlein (U.S. Patent No. 6,097,625). Claim 39 also stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Durlam, et al., in view of Baek et al. (U.S. Patent No. 5,843,837).

These rejections are respectfully traversed in the following discussion.

I. THE CLAIMED INVENTION

The claimed invention (as recited in claim 11) is directed to an array of microelectronic elements which includes a substrate of semiconductor material, a lower layer of dielectric material disposed with a lower surface in contact with the substrate and an upper surface in spaced adjacency thereto, a pattern of mutually electrically isolated conductive regions disposed within the lower layer of dielectric material, the conducting regions extending to the upper surface of the lower layer, an upper layer of dielectric material disposed with a lower surface thereof in contact with and bonded to the upper surface of the lower layer, and a plurality of nodes of semiconductor material disposed within the upper layer of dielectric material, each of the nodes being in electrical contact with only one of the

conducting regions at the upper surface of the lower layer.

Importantly, each conducting region includes a metal conductor, and a via which is filled with a diffusion barrier material, the diffusion barrier material extending between the metal conductor and a node in said plurality of nodes and electrically connecting the metal conductor with the node.

Conventional devices typically form a semiconductor node (e.g., a silicon diode) directly on an aluminum or copper metal conductor (e.g., a word line). **For example, this is clearly shown in Figure 17 of the Durlam reference, which shows a diode 93 formed on a metal conductor 82 which is formed of Al or Cu.**

However, such devices **such as that shown in Figure 17 of Durlam** suffer severe problems. Namely, **the metal conductor reacts with the semiconductor node, thereby making the devices unreliable.**

To address this problem, the metal conductor (e.g., word line) may be made from a refractory metal. However, such refractory metal word lines have a high resistance, such that only small arrays of memory elements can be made (Application at page 8, lines 10-13).

The claimed invention, on the other hand, includes a via formed on the metal conductor and filled with a diffusion barrier material which extends between the metal conductor and a node in the plurality of nodes and electrically connects the metal conductor with the node. The diffusion barrier material keeps the conductive region from reacting with the semiconductor material in the node. Therefore, the word lines can be formed of a low resistance metal such as copper and aluminum, for improved performance.

II. THE PRIOR ART REFERENCES

A. The Durlam Reference

The Examiner alleges that Durlam teaches the claimed invention as recited in claims 11-12, 15-16, 18, 26, 28-29, 33-35 and 36-38. Applicant submits, however, that there are elements of the claimed invention which are neither taught nor suggested by Durlam.

Contrary to the Examiner's allegations, Durlam does not teach or suggest a conductive via which includes a "*a via which is filled with a diffusion barrier material, said diffusion barrier material extending between said metal conductor and a node in said plurality of nodes and electrically connecting said metal conductor with said node*" as recited, for

example, in claim 11 and similarly recited in claims 26 and 38.

As noted above, conventional devices **such as that shown in Figure 17 of Durlam** suffer severe problems. Namely, **the metal conductor reacts with the semiconductor node, thereby making the devices unreliable.**

The claimed invention, on the other hand, includes a via formed on the metal conductor and filled with a diffusion barrier material which extends between the metal conductor and a semiconductor node and electrically connects the metal conductor with the semiconductor node. (Application at page 8, lines 3-16; Figure 5B). The diffusion barrier material keeps a metal conductor (e.g., word line) from reacting with the semiconductor material (e.g., silicon diode). Therefore, the word lines can be formed of a low resistance metal such as copper and aluminum for improved performance (Application at page 8, lines 3-16).

Clearly, Durlam does not teach or suggest these novel features. Indeed, Durlam does not even discuss at least one of the problems (e.g., reaction between a semiconductor node and a metal conductor (e.g., a word line)) which the claimed invention was intended to address.

The Examiner attempts to rely on Figures 5-8 in Durlam to support his allegations. Specifically, the Examiner **surprisingly** attempts to equate the metal conductor 37 in Durlam with the via in the conducting region of the claimed invention (e.g., via 13 in the exemplary embodiment illustrated in Figures 5A-5B of the Application). However, the Examiner is completely incorrect.

In particular, the Examiner relies on col. 3, lines 35-42 to support his allegation that the via includes Ta (e.g., a diffusion barrier material). However, this passage merely refers to Figure 3, stating:

> "In order to improve adhesion of field focusing layer 24 and to provide a barrier for Ni or Fe diffusion into the conductor and/or dielectric a layer of Ta or TaN or such materials could be added **between field focusing layer 24 and conductor layer 26**" (Durlam at col. 3, lines 39-42) (emphasis added).

Applicant notes that conductor layer 26 eventually becomes the metal conductor 37

illustrated in Figure 5 in Durlam. Therefore, Durlam merely teaches that a "barrier" may be provided **before forming the metal conductor 37**. That is, nowhere does this passage or Figure 3 in Durlam teach or suggest that the metal conductor 37 includes barrier material.

It is **also important to note that Durlam teaches that the conductor line 45 (which the Examiner surprisingly attempts to equate with the node in the claimed invention) directly contacts the conductor 37**. That is, even assuming that a refractory metal layer is formed beneath the conductor 37, the conductor line 45 still contacts mostly the conductor 37which does not include any refractory metal. Thus, this embodiment of Durlam clearly does not teach or suggest the importance of separating a node from an aluminum/copper conductor in order to avoid any interaction between the a node and an aluminum/copper conductor.

Moreover, even if is it assumed (arguendo) that the metal conductor 37 includes a diffusion barrier material, the metal conductor 37 still cannot reasonably be equated with the via of the claimed invention. Indeed, as recited in claim 11, in the claimed invention, the via extends between the metal conductor and a semiconductor node and electrically connects the metal conductor with the semiconductor node. (Application at page 8, lines 3-16; Figure 5B). In fact, the via in the claimed invention may be used to prevent the metal conductor from reacting with a semiconductor node, such as a silicon diode.

Durlam, on the other hand, teaches that the metal conductor 37 is used to "electrically connect plug conductors 19a and 19b to conductor layer 34" (Durlam at col. 3, line 67). That is, the metal conductor 37 electrically connects the plug conductors 19a, 19b to the metal conductor layer 45, as illustrated in Figure 7 (e.g., see Durlam at Abstract). Therefore, the function of the metal conductor 37 is completely different that the function of the via in the claimed invention.

For example, in the exemplary embodiment illustrated in Figure 5A, the via includes a diffusion barrier material which extends between the word line 15 and a diode mesa including Si layer 3'. Thus, the via may be used to electrically connect the metal conductor with the semiconductor node.

In fact, the Examiner expressly concedes that the portion of Durlam on which he is relying as disclosing the claimed invention, does not teach or suggest this feature. However, the Examiner **surprisingly refers to a completely unrelated aspect of Durlam** as allegedly

disclosing this feature. Specifically, the Examiner alleges that this feature is disclosed in Figure 17 of Durlam which is completely unrelated to the embodiment in Figure 5 of Durlam.

Moreover, Figure 17 in Durlam teaches forming a semiconductor diode in direct contact with an aluminum/copper conductor. Applicant would respectfully point out that the present Applicant expressly teaches that such a device is not reliable. Indeed, that is one of the problems which the claimed invention is intended to solve.

Applicant would respectfully submit that it is absolutely unreasonable for the Examiner to attempt to rely on Figure 17 in Durlam as somehow teaching the claimed invention, when Figure 17 expressly teaches one of the very problems (e.g., reaction between an Al/Cu layer and a semiconductor) which the claimed invention was intended to solve.

Indeed, an important point for the Examiner to consider is that Durlam clearly does not teach or suggest the importance of forming a diffusion barrier between a metal conductor an a semiconductor node, which is an important feature of the claimed invention. Indeed, Durlam specifically teaches that it is desirable to form a semiconductor directly in contact with the metal conductor. That is, Durlam teaches away from the teachings of the claimed invention.

Further, Applicant respectfully reminds the Examiner that he **must read the Durlam reference as a whole**. He can not merely search throughout the reference willy-nilly, and picking and choosing unrelated features to somehow kluge together a basis for his unreasonable rejection. In this instance, the Examiner is surprisingly relying on alleged features from completely unrelated and different aspects to support his position, which cannot form the basis for his rejection. Clearly, the embodiment of Figure 17 would not have been combined with the unrelated embodiment of Figure 5, and the Examiner has failed to provide any adequate motivation or suggestion for such combination.

Indeed, the Examiner merely states that these embodiments would have been combined "for the purpose of switching a magnetic memory element to read information in the magnetic memory element" which does not explain any motivation or suggestion to combine these embodiments.

Moreover, even assuming that the embodiment of Figure 17 would have been combined with the embodiment of Figure 5, the alleged combination would not teach or

suggest a conductive via which includes a via formed on the metal conductor and filled with a diffusion barrier material which extends between the metal conductor and a semiconductor node and electrically connects the metal conductor with the semiconductor node.

Indeed, Figure 17 does not even teach or suggest a "via" as in the claimed invention, but instead illustrates **a diode 95 formed directly on a metal conductor 82.** Certainly, Figure 17 does not teach or suggest a via which is filled with a diffusion barrier material extending between a metal conductor and a semiconductor node.

Therefore, contrary to the Examiner's allegations, nowhere does Durlam teach or suggest the conductive via of the claimed invention.

Therefore, Applicant submits that there are elements of the claimed invention that are not taught or suggest by Durlam. Therefore, the Examiner is respectfully requested to withdraw this rejection.

B. The Bronner Reference

The Examiner alleges that Durlam would have been combined with Bronner to form the claimed invention as recited in claims 13-14, 17, 27 and 30-31. Applicant submits, however, that these references would not have been combined and even if combined, the combination would not teach or suggest each and every element of the claimed invention.

Specifically, neither Durlam, nor Bronner, nor any combination thereof teaches or suggests "*a via which is filled with a diffusion barrier material, said diffusion barrier material extending between said metal conductor and a node in said plurality of nodes and electrically connecting said metal conductor with said node*" as recited, for example, in claim 11 and similarly recited in claims 26 and 38.

As noted above, conventional devices such as that shown in Figure 17 of Durlam suffer severe problems. Namely, the metal conductor reacts with the semiconductor node, thereby making the devices unreliable.

Clearly, Bronner does not teach or suggest these novel features. Indeed, Bronner does not even discuss at least one of the problems (e.g., reaction between a semiconductor node and a metal conductor (e.g., a word line)) which the claimed invention was intended to address.

Further, Applicant notes that the Examiner merely relies on Bronner as allegedly

disclosing a single crystal Si diode. That is, the Examiner is not relying on Bronner as disclosing the novel features of the claimed invention.

In addition, Bronner merely discloses a diode 514 which is in the shape of a V-groove formed in an insulation layer100. A metal conductor 525 is formed on the diode 514 and an oxide layer 530 is formed on the metal conductor 525 (Bronner at Figure 5B). This structure is completely unrelated to the claimed invention.

Therefore, Bronner clearly does not teach or suggest a via formed on the metal conductor and filled with a diffusion barrier material which extends between the metal conductor and a node in the plurality of nodes and electrically connects the metal conductor with the node. Thus, Bronner clearly does not make up for the deficiencies of Durlam.

Therefore, Applicant submits that these references would not have been combined and even if combined, the combination would not teach or suggest each and every element of the claimed invention. Therefore, the Examiner is respectfully requested to withdraw this rejection.

C. The Scheuerlein and Baek References

The Examiner alleges that either Scheuerlein of Baek would have been combined with Durlam to form the claimed invention as recited in claims 39. Applicant submits, however, that these references would not have been combined and even if combined, the combination would not teach or suggest each and every element of the claimed invention.

Specifically, neither Scheuerlein, nor Baek, nor Durlam, nor any combination thereof teaches or suggests *"a via which is filled with a diffusion barrier material, said diffusion barrier material extending between said metal conductor and a node in said plurality of nodes and electrically connecting said metal conductor with said node"* as recited, for example, in claim 11 and similarly recited in claims 26 and 38.

As noted above, conventional devices such as that shown in Figure 17 of Durlam suffer severe problems. Namely, the metal conductor reacts with the semiconductor node, thereby making the devices unreliable.

Clearly, neither Scheuerlein nor Baek teach or suggest these novel features. Indeed, neither of these references even discuss at least one of the problems (e.g., reaction between a semiconductor node and a metal conductor (e.g., a word line)) which the claimed invention

was intended to address.

The Examiner attempts to rely on Figure 6 and col. 5, lines 1-8 in Scheuerlein, and Figure 1C and col. 2, lines 52-54 in Baek to support his position.

However, nowhere do these drawings or passages (nor anywhere else for that matter) teach or suggest the importance of forming a diffusion barrier material between a metal conductor and a node (e.g., semiconductor material).

Therefore, neither Scheuerlein nor Baek teach or suggest a via formed on the metal conductor and filled with a diffusion barrier material which extends between the metal conductor and a node in the plurality of nodes and electrically connects the metal conductor with the node. Therefore, these references clearly do not make up for the deficiencies of Durlam.

Therefore, Applicant submits that these references would not have been combined and even if combined, the combination would not teach or suggest each and every element of the claimed invention. Therefore, the Examiner is respectfully requested to withdraw this rejection.

III. FORMAL MATTERS AND CONCLUSION

In view of the foregoing, Applicant submits that claims 11-18 and 26-31 and 33-43, all the claims presently pending in the application, are patentably distinct over the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary in a telephonic or personal interview.

The Commissioner is hereby authorized to charge any deficiency in fees or to credit any overpayment in fees to Assignee's Deposit Account No. 50-0510.

Respectfully Submitted,

Date: 9/30/04

Phillip E. Miller
Registration No. 46,060

McGinn & Gibb, PLLC
8321 Old Courthouse Road, Suite 200
Vienna, VA 22182-3817
(703) 761-4100
Customer No. 21254

CERTIFICATE OF FACSIMILE TRANSMISSION

I hereby certify that the foregoing Amendment was filed by facsimile with the United States Patent and Trademark Office, Examiner Phat X Cao , Group Art Unit # 2814 at fax number (703) 872-9306 this 30th day of September, 2004.

Phillip E. Miller
Reg. No. 46,060